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DOCKET NO. 91-C-127C1 (STMI01-00022) **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Jia Li

U.S. Serial No. : 09/803,715

Filed : March 9, 2001

For : METHOD OF FORMING ACTIVE AND ISOLATION AREAS WITH SPLIT ACTIVE PATTERNING

Group No. : (Not Yet Known)

Examiner : (Not Yet Assigned)

Commissioner of Patents
and Trademarks
Washington, D. C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 6/26/01.

KATHY LONGENECKER
(Printed/or typed name of person signing the certificate)

Kathy Longenecker
(Signature of the person signing the certificate)

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

U.S. Patent No.	Inventor	Date
4,829,019	Mitchell, et al.	May 9, 1989

Foreign Patent No.	Country	Date
0123384	Europe	Oct. 31, 1984
0065445	Japan	April 13, 1984
0050634	Japan	April 12, 1980
0271956	Japan	Nov. 9, 1988
0189208	Europe	July 30, 1986
0275508	Europe	July 27, 1988
0208935	Europe	Jan. 21,1987
WO 83/02197	PCT	June 23, 1983
0401174	Europe	Dec. 5, 1990

Other References

"Silicon Processing for the VLSI Era," Vol. 2: Process Integration by Stanley Wolf, Ph.D.,1990, pp. 38-41.

International Electron Devices Meeting, December, 1982, Washington, D.C. - "Electrical Properties of MOS Devices Made with Silo Technology," J. Hui, T.Y. Chiu, S. Wong and W.G. Oldham, IEEE, 1982, pp. 220 - 223.

International Electron Devices Meeting, December 8, 1980, Washington, D.C.- "Selective Polysilicon Oxidation Technology for Defect Free Isolation, Junichi Matsunaga, Naohiro Matsukawa, Hiroshi Nozawa, and Susumu Kohyama, IEEE, 1980, pp. 565-568.

"Under Field Oxide Dopant Enhancement (UFDE) for CMOS and BiCMOS Technology," Extended Abstracts of the 22nd (1990) International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 649-652.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

NOVAKOV DAVIS & MUNCK, P.C.

Date: 6-26-01

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